teaches the best mode known by Applicant for contacting his gate. To better explain why the present specification teaches how to contact the polysilicon gate, reference is made to Figures A to D, attached hereto. Figure A illustrates a portion of the semiconductor wafer at the point during the manufacturing process illustrated by Figure 4c of the Application. Thus, although Figure 4c illustrates groove 31* in two dimensions, as illustrated in attached Figure A, it is seen that groove 31* extends in a direction indicated by arrow Z. Referring to Figure B (which illustrates the wafer at the point during manufacturing illustrated by Figure 4d of the Application), polycrystalline silicon layer 33 is then formed on the wafer surface. Thereafter, a photomask M is formed on polysilicon layer 33. Mask M is described in the specification as follows:

> A mask (not shown) . . . may be placed at any convenient point along the length of groove 31 in order to keep a contact pad (not shown) to the to-be-formed gate 34 shown in Fig. 4e . . . . (Page 6, lines 23 to 26.)

The specification also indicates that "polycrystalline silicon layer 33 is then subjected to a CF_4 etch or another etch technique . . . ." (Page 6, lines 21 to 22.) Figure C illustrates the resulting structure. Thereafter, mask M is removed. (See Figure D.) As can be seen, the polysilicon 33 includes a portion which extends out of groove 31* and onto the wafer surface. This portion of polysilicon 33 is then easily electrically contacted. Thus, as can be seen in attached Figures A to D, the specification clearly teaches one of ordinary skill in the art how to contact polysilicon 33. If the Examiner has further questions regarding the manner by which polysilicon 33 is contacted, the Examiner is respectfully requested to phone Applicant's attorney at (408) 246-1405.

The Examiner has rejected Claims 8 to 16

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> under 35 U.S.C. 103 as being unpatentable over Schutten et al. in view of Arnould et al. Schutten et al. discloses a method of making power semiconductor device by filling insulator lined U-groove with conductor material. (See Fig. 2, 13, and col. 6, lines 57+, and col. 4, lines 1-41.) Schutten et al. lacks anticipation only in not forming insulator layer over the conductive gate filler.

The Examiner has also rejected Claims 8 to 16 "under 35 USC 103 as being unpatentable over admitted prior art in view of Iwai, Furumaura (sic), and Arnould et al." Applicant has amended Claims 8, 10 and 12 and has added Claim 17, thereby overcoming the above rejections.

APPLICANT HAS OVERCOME THE REJECTION OF CLAIMS 8 TO 12

Applicant's Claim 8 includes the step of

> forming an insulating layer having a planar top surface over the device resulting from the preceding steps, the thickness of the portion of said insulating layer over said conductive material being greater than the thickness of the portion of said insulating layer over said third region.

Nowhere does the cited art teach or even suggest such a structure. Schutten Fig. 13 at first glance appears to illustrate a transistor including a conductive gate having a planar top surface formed in a groove. (Actually, Schutten Fig. 13 is merely a schematic illustration and, in fact, the structure actually taught by Schutten has an appearance different from that of Fig. 13.) In any event, Schutten fails to teach or even suggest forming an insulating layer on the surface of his transistor such that "the thickness of the portion of said insulating layer over said conductive material (is) greater than the thickness of the portion of said insulating layer over said third region." Therefore, Schutten fails to render obvious Applicant's claimed invention.

The above distinction is important. Because Applicant forms a thicker oxide over polysilicon 34 (Applicant's Fig. 4f)

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than over N+ source regions 21a and 21b, when Applicant etches his insulation layer 30 to permit electrical contact to the source region, Applicant can use a blanket etching process. Therefore, Applicant does not have to allow for misalignment between a source body contact mask and the gate region. Thus, Applicant can form his transistor using a smaller surface area than would be required if Applicant had to use a photomask to prevent etching of silicon dioxide over polysilicon gate 34. Nowhere does Schutten teach or suggest such an advantage. Therefore, Schutten fails to render obvious Applicant's claimed invention.

Arnould merely discusses a polysilicon structure formed in a groove which electrically contacts a subsurface doped region in a semiconductor wafer. It is not clear to Applicant's attorney what Arnould seeks to accomplish with his structure. However, it is clear that Arnould neither teaches nor suggests Applicant's claimed invention which includes the step of

> filling the bottom portion of said second, inner groove with a conductive material so that a top surface of said conductive material in said second, inner groove lies between said first portion and said second portion of said third region, said conductive material serving as a gate. . . . (Applicant's Claim 8.)

Nowhere does Arnould teach or even suggest that his polysilicon 15 should serve as a gate. Therefore, Arnould fails to render obvious Applicant's claimed invention. Further, because the Arnould conductive polysilicon 15 does not serve as a gate, Arnould fails to teach or suggest

> forming an insulating layer having a planar top surface over the device resulting from the preceding steps, the thickness of the portion of said insulating layer over said conductive material (which serves as a gate) being greater than the thickness of the portion of said insulating layer over said third region. (Applicant's Claim 8.)

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Therefore, Arnould combined with Schutten fails to render obvious Applicant's claimed invention.

Applicant points out that because Arnould polysilicon 15 is not a gate, the design considerations which cause Arnould to manufacture his structure in the manner described are different from those faced during the construction of Applicant's transistor. For example, Arnould is not faced with the problem of minimizing the distance between a source body contact area such as the area where Applicant's metallization 18 (Fig. 3) contacts N+ regions 21a and 21b and the edge of the groove. Thus, Arnould does not suggest Applicant's invention to one of ordinary skill in the art for this reason as well.

Furumura is in Japanese, and thus, Applicant is unsure of the contents. However, the Furumura English language abstract also fails to teach or suggest forming insulating material over a gate formed in a groove such that the insulating material over the gate is thicker than the insulating material over the rest of the device. Iwai similarly fails to teach or suggest such a process step. Because Furumura, Iwai, Schutten and Arnould each fail to show this feature, these references combined fail to render obvious Applicant's claimed invention.

Schutten further fails to render obvious Applicant's claimed invention (alone or in combination with any of the other references) because Schutten Fig. 13 is merely a schematic illustration of the Schutten structure, and in fact the device that Schutten actually forms has an appearance completely different from that illustrated in Schutten Fig. 13. Thus, Schutten indicates that "FIG. 13 is a schematic sectional view of completed FET structure constructed in accordance with the invention. FIGS. 14 through 21 show the preferred processing and structure of the invention." (Schutten Col. 3, lines 16 through 20.) Schutten further states "FIGS.

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12 and 13 schematically show lateral bidirectional power FET structure constructed in accordance with the invention." (Schutten Col. 6, lines 57 to 59, emphasis added.) Schutten again states "FIGS. 14 through 21 show the preferred processing and structure of the invention." (Schutten Col. 9, lines 67 to 68.) As can be seen in Figs. 14 through 21, the actual Schutten structure (see Fig. 21) does not resemble Applicant's claimed invention. For example, in the process described by Schutten, he does not fill the bottom portion of his groove with conductive material and then form an insulating layer "having a planar top surface" over his transistor as set forth in Applicant's Claim 8. Therefore, Schutten fails to render obvious Applicant's claimed invention for this reason as well.

APPLICANT HAS OVERCOME THE REJECTION OF CLAIM 12

Applicant's Claim 12 recites the steps of

> filling the bottom portion of said second, inner groove but not the top portion of said second, inner groove with a conductive material so that a top portion of said conductive material in said, inner groove lies adjacent to the portion of said dielectric material adjacent to said third region. . . . (and)
>
> forming an insulating layer having a planar top surface over the device resulting from the preceding steps, wherein the portion of the insulating layer over said conductive material is thicker than the portion of the insulating layer over said third region . . . .

Thus, Applicant claims a step such as illustrated in Figure 4e wherein the polysilicon in the upper portion of the groove has been removed. This is an important distinction. Because the conductive gate does not reach the top surface of the groove in the vicinity of the cross section of Figure 4e, it is not necessary to leave a significant amount of space between the edge of the area where source and body contact metallization 18 contacts regions 21a and 21b (Application Fig. 3) and the edge

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of the groove. Thus, the transistor can be constructed on a smaller surface area than if the gate extended to the groove surface in the vicinity of the cross section of Fig. 3. In contrast to the structure of prior art Fig. 2 of the Application, in which a significant amount of space must be left between groove 23 and the area where metallization 18 contacts regions 21a and 21b, in the structure of Applicant's Figure 3 and Claim 12, the space between the groove and source body contact area be minimized. Nowhere does Schutten teach or even suggest such a structure. Schutten Figures 14 to 21 do not teach or suggest a transistor having a cross section in which the gate material at the top of a groove has been removed. In fact, Schutten's gate extends outside of his groove in the cross section of Figure 21, and thus Schutten does not provide the above-mentioned advantage.

Schutten Figure 13 (which as mentioned above, does not accurately depict the structure that Schutten actually teaches) illustrates a gate that is coplanar with the top of his wafer. Thus, Schutten Figure 13 also fails to teach or suggest Applicant's Claim 12.

As mentioned above, Arnould does not pertain to the formation of a gate, and there is nothing in Arnould to suggest to one of ordinary skill in the art that one could form a gate as claimed by Applicant. Arnould forms his polysilicon structure to serve as a contact for a subsurface doped region, and not as a gate.

Iwai illustrates a gate extending to the surface of a groove (see Iwai Figure 4e). Iwai also states that the gate material can be etched so that the top surface of the gate is recessed relative to the surface of the wafer surface. (See Iwai Fig. 5 and accompanying text on Column 5, lines 42 to 49.) However, while Iwai mentions that his gate can be etched

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to be recessed relative to the transistor surface, Iwai does not teach or suggest that "the portion of the insulating layer over (his gate) is thicker than the portion of the insulating layer over (his source or body region)." Thus, there is no clear teaching in Iwai of a process in which a blanket etching process could be used to extend the source contact area to the edge of a groove, thereby minimizing transistor surface area. (The recessed gate structure alone, without the presence of insulation over the gate which is thicker than the insulation over the source, will not enable one to use a blanket etching process to define the source contact.) Thus, Iwai fails to teach or render obvious Applicant's claimed process, which provides the advantage of permitting the use of a blanket etching process to define the source contact area, thereby permitting a smaller transistor surface area.

Applicant also points out that Iwai fails to indicate any benefit for forming a gate having a recessed top surface. Thus there is no suggest in the prior art to combine the recessed gate feature of Iwai with any of the other references.

APPLICANT'S CLAIM 17 IS PATENTABLE OVER THE CITED ART

Applicant's Claim 17 is directed toward a method for making a vertical multicell transistor in which the source is contacted on the top surface of the transistor and the drain is contacted on the bottom surface of the transistor. The transistor includes a groove extending through the source and body regions of the transistor cells. (Applicant uses a multicell structure to enable the transistor to conduct large amounts of current in high power applications. See Figure 9 of the application.) A conductive gate is formed which fills the bottom of the groove, and an insulating layer having a planar top surface is formed over the gate.

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Iwai merely discusses a lateral single cell transistor (not a vertical multicell transistor). This distinction is extremely significant. Attached hereto is a Declaration demonstrating that Applicant achieves significant savings in surface area by forming the gate in the claimed manner in a multicell transistor. In fact, in Applicant's transistor, Applicant can save thousands of microns in one dimension by manufacturing his transistor in the claimed manner.

Because Iwai's transistor does not achieve such significant size reductions, one of ordinary skill in the art, reading Iwai, would not realize that such a saving in transistor surface area could be realized. Thus, Iwai fails to render obvious Applicant's claimed invention.

The Furumura abstract fails to teach a multicell transistor. Further, Furumura discusses a lateral transistor, i.e. his source and drain are contacted at the transistor top surface instead of contacting the drain at the bottom surface as recited in Applicant's Claim 17. Thus, Furumura's device is fundamentally different from Applicant's device, and does not achieve the advantages of Applicant's device.

Schutten and Arnould similarly fail to teach a structure achieving the advantages described in the attached Declaration. Thus, Applicant's invention is patentable over Schutten, Arnould, Iwai and Furumura, combined.

INFORMATION DISCLOSURE STATEMENT

Pursuant to Rule 37 C.F.R. 1.56, Applicant wishes to bring to the Examiner's attention the following references:

U.S. Patent 4,398,339, issues to Blanchard et al.;

U.S. Patent 4,639,754, issues to Wheatley, Jr., et al.;

Japanese Patent Publication 53-149771, assigned to Matsushita;

Japanese Patent Publication 55-146976, filed by Hideshima;

returned copy PTO-1449 dated 11-25-87 MFO

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Article by Baliga et al. entitled "The Insulated Gate Transistor: A New Three-Terminal MOS-Controlled Bipolar Powered Device", published in IEEE Transactions On Electron Devices June 1984.

Article entitled "A New Vertical Power MOSFET Structure With Extremely Reduced On-Resistance" published in IEEE Transactions On Electron Devices January 1985.

Each of the above-mentioned reference was cited during prosecution of U.S. Patent Application No. 06/929,685 filed November 13, 1986, which is a divisional patent application of the present patent application. Applicant requests that these references be made of record in the present application, as well.

In the above-mentioned divisional application, the Examiner also cited Japanese patent document 0097442 filed by Schutten and U.S. Patent 4,344,081 issued to Pao et al. Applicant does not presently have a copy of the 0097442 document or the '081 patent.

Applicant also brings to the Examiner's attention the following references.

U. S. Patent 4,682,405, issued to Blanchard et al. on July 28, 1987. Blanchard teaches forming an insulating layer 120 (Figs. 2c and 2d) on a to-be-formed transistor. The portion of insulation 120 over gate 112 is thicker than the portion of insulation 120 over N+ source 116. The portion of insulation 120 over N+ source 116 is then removed using a blanket etching step (See column 4, lines 15 to 24). The '405 patent fails to teach a planar transistor structure and therefore fails to render obvious Applicant's claimed invention.

"Deep Trench Isolated CMOS Devices" by Rung et al. discusses the formation of polysilicon-filled trenches surrounding lateral MOS transistors in CMOS integrated circuits to prevent parasitic SCR latch-up. Rung forms 4000A thick SiO_2 over the polysilicon in his groove. However, the polysilicon in Rung's groove does not serve as a gate, nor does Rung seek

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to minimize the distance between a source/body contact area and the polysilicon in his groove.

As Applicant has overcome each of the rejections set forth by the Examiner, Applicant respectfully submits that Claims 8 to 17 are in condition for allowance. If the Examiner's next action is other than allowance, the Examiner is respectfully requested to telephone Applicant's attorney at (408) 246-1405.

Respectfully submitted,

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Attorney for Applicant
Reg. No. 30,566

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, November 23, 19 87.

November 23 1987
Date of Signature

Attorney for Applicant

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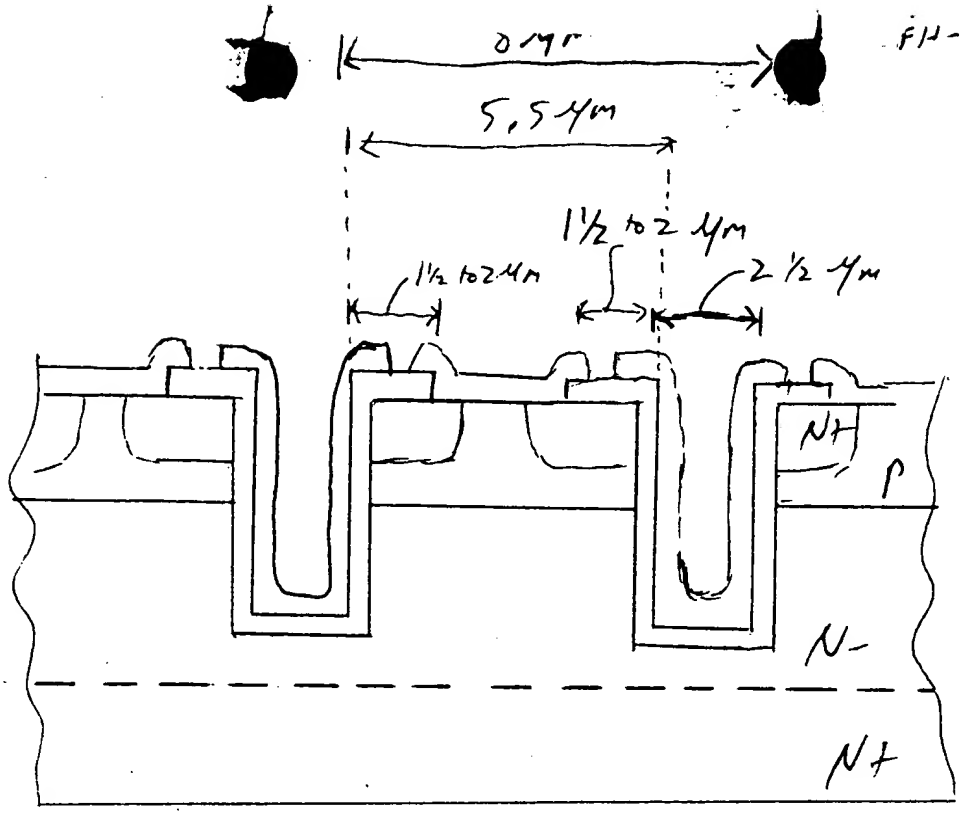

FIGURE A

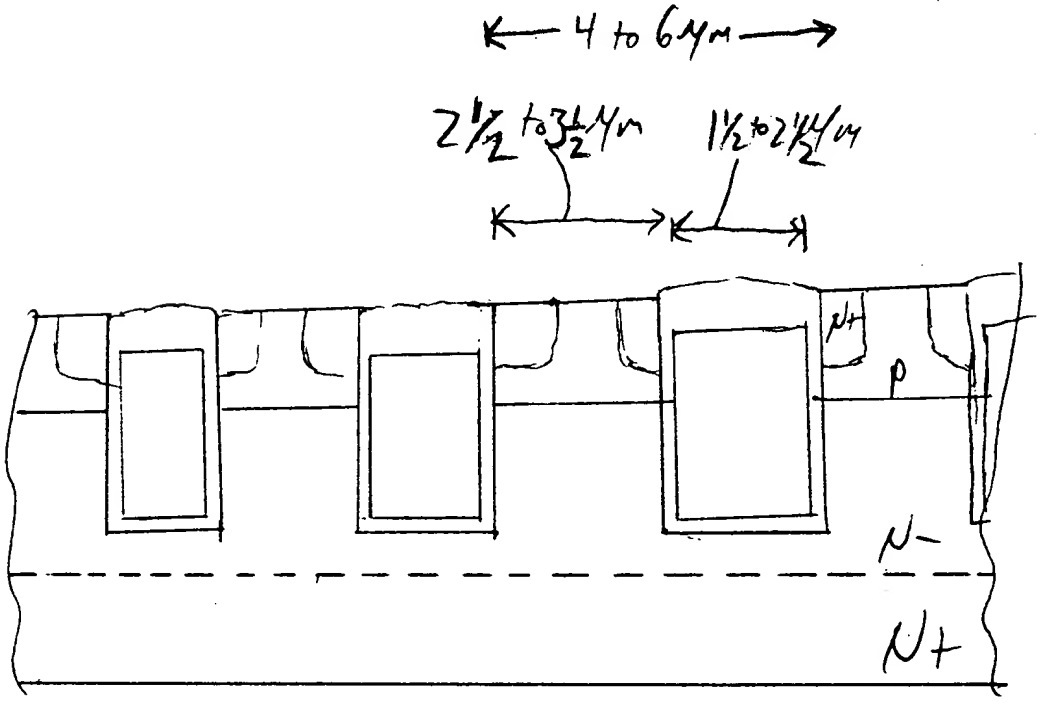

FIGURE B.

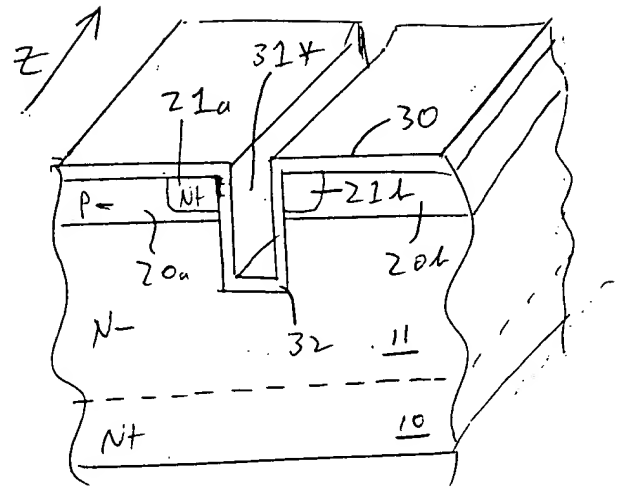
Z
31
21a
30
P-
N+
21
20a
20
N-
32
11
N+
10

FIG. A

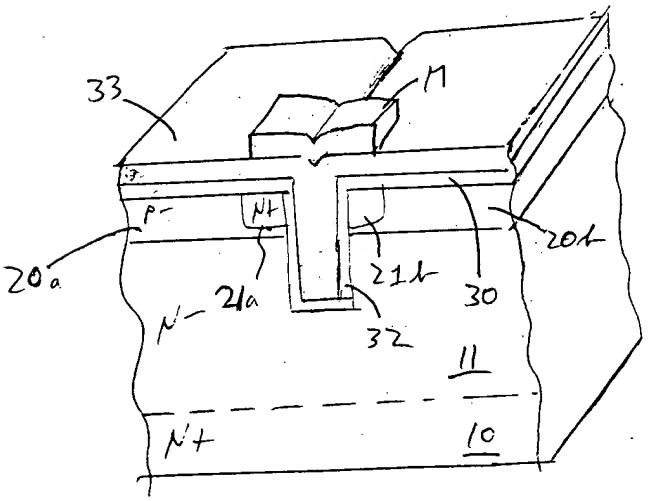
33
M
P-
N+
20a
21a
21
30
20
N-
32
11
N+
10

FIG. B

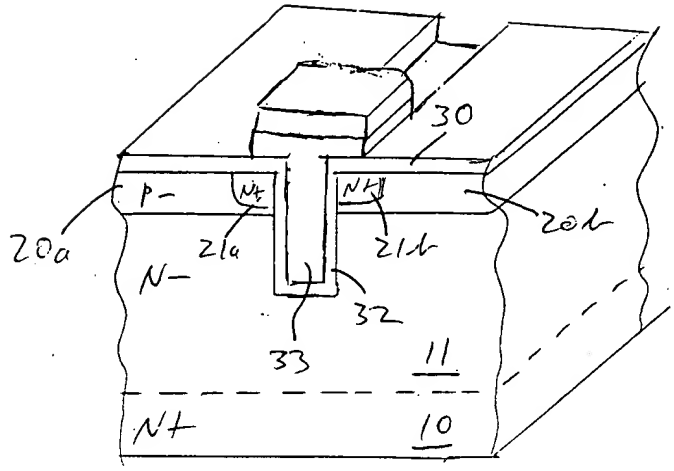
30
P-
N+
N+
20a
21a
21b
20b
N-
32
33
11
N+
10

FIG C

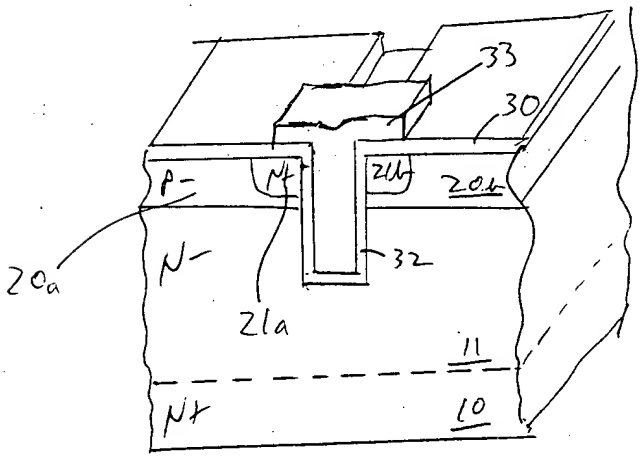
33
30
P-
N+
21b
20b
20a
N-
32
21a
11
N+
10

FIG. D.